Vision processors

Matrox **Odyssey Xpro+**

Scalable vision processor board with customizable co-processor FPGA.

Key features

- PCI-X long card
- G4 PowerPC™, proprietary ASIC and customizable co-processor FPGA
- over 5 GB per second of memory bandwidth
- up to 2 GB of DDR SDRAM memory
- up to 2 GB per second of external I/O bandwidth
- PMC site for optional frame grabber module
- Camera Link® frame grabber module acquires up to 680 MB per second
- quad-input analog frame grabber module acquires up to 800 MB per second
- pair of dedicated board-to-board interconnects each capable of up to 1 GB per second
- available software is sold separately and includes Matrox Imaging Library (MIL)[1] and Matrox Odyssey Developer's Toolkit
- host OS support for 32/64-bit Microsoft® Windows® XP/Vista®/7 and 32-bit Linux®
- royalty-free redistribution of MIL and ONL run-time environments[1]

Balanced architecture with unprecedented performance

Matrox Odyssey Xpro+ represents the culmination of vision processor board design. This enhanced fourth generation vision processor board combines the latest off-the-shelf and custom technologies in a truly balanced architecture to deliver unprecedented levels of performance and value. Designed with demanding semiconductor inspection, medical imaging, print inspection, surface inspection and signal processing applications in mind, the Matrox Odyssey Xpro+ is the ideal choice for applications with data acquisition and processing rates in the order of hundreds of MBytes per second and/or where the PC is heavily loaded with other system activities.

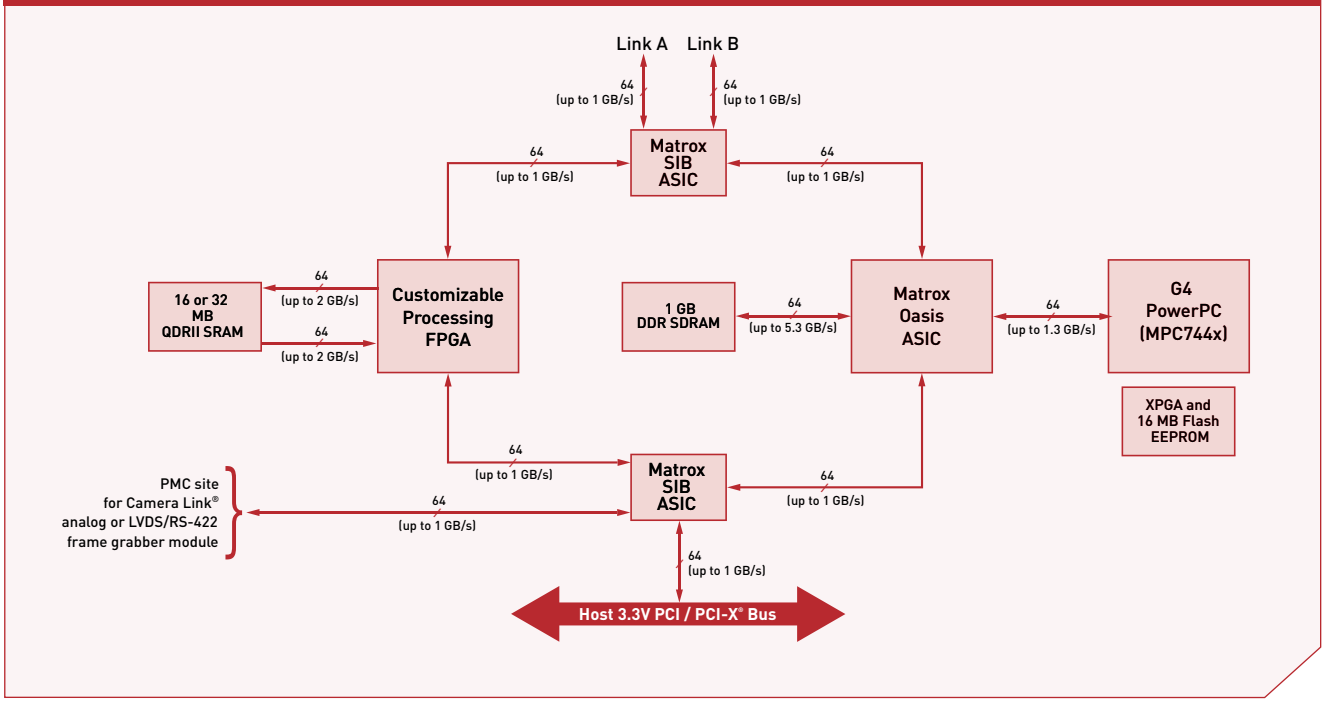
The premier embedded microprocessor, state-of-the-art proprietary processor and router ASICs, customizable co-processor FPGA, DDR memory, and PCI-X® interconnectivity come together on the Matrox Odyssey Xpro+ to provide unrivaled power for a single vision processor board. Additionally, the Matrox Odyssey Xpro+ is ready to expand to meet today and tomorrow's processing requirements with its linearly scalable architecture. All this power and flexibility is accessed through an easy-to-learn programming environment compatible with Matrox Imaging's previous generation vision processor and incorporating elaborate image processing and analysis algorithms.

State-of-the-art Matrox Oasis ASIC

The Matrox Imaging designed Oasis ASIC is the pivotal component of the Matrox Odyssey Xpro+. A high-density chip, the Matrox Oasis integrates a CPU bridge, Links Controller, main memory controller and Pixel Accelerator.

MATROX
IMAGING

Matrox Odyssey Xpro+



Pixel Accelerator

The Pixel Accelerator (PA) is a parallel processor core, which considerably accelerates neighborhood, point-to-point and LUT mapping operations. It consists of an array of 64 processing elements all working in parallel. Each processing element has a multiply-accumulate (MAC) unit and an arithmetic-logic unit (ALU).

The MAC unit is capable of performing a single 16-bit by 16-bit, two 8-bit by 16-bit or four 8-bit by 8-bit multiplies with 40-bit accumulation per cycle for convolution operations. The 40-bit accumulator guarantees no overflow situation for a 16 by 16 kernel with 16-bit coefficients and data. In addition, the PA architecture allows symmetrical kernels to be processed four times faster. The MAC unit is also able to perform up to four minimum or maximum operations per cycle for grayscale morphology operations.

The ALU can execute a wide variety of arithmetic and logical operations. It can be programmed to execute a sequence of 256 instructions per pixel at one instruction per cycle reducing the amount of memory accesses and further accelerating memory I/O-bound sequences. The PA can accept up to four source buffers[2] and output to four destination buffers allowing several operations to be performed at once or in a single pass (e.g., four images can be averaged in one pass). Operating at a core frequency of 167 MHz enables the PA to carry out up to 100 BOPS[3] (i.e., process up to two billion pixels per second).

Memory controller

The Matrox Oasis includes a very efficient main memory controller for managing the 128-bit wide interface to DDR SDRAM. Operating at 167 MHz, the DDR SDRAM and controller combine to deliver
a memory bandwidth in excess of 5 GB per second. Such ample memory bandwidth allows the Odyssey Xpro+ to comfortably handle demanding video I/O while maintaining PA performance even for memory I/O-bound operations.

Links Controller

The Links Controller (LINX) is the router that manages all data movement inside and outside the processing node, which consists of the PA, CPU and main memory. It can handle several concurrent video and message streams.

Video streams are used to transfer image data from one or more frame grabber modules to one or more processing nodes, between processing nodes, and from one or more processing nodes to the host PC and display. The video streams have adjustable priority levels, either above or below message streams. Video streams can be subject to various formatting operations including plane separation on input and merging on output, input cropping, input and output sub-sampling (1 to 16), and independent control of horizontal and vertical scanning direction. The latter is particularly useful for reconstructing a proper image from a camera whose readout requires multiple taps, each with different scanning directions.

Message streams are for all types of inter-processor communications. The LINX handles message streams between a processing node and the host PC or other processing nodes independently of video streams. Message passing relies on hardware-assisted mechanisms for low overheads and real-time operation. Together, the above capabilities off-load the CPU and PA from data management tasks so they can focus on image processing tasks.

Customizable co-processor FPGA

For operations not accelerated by the PA, Matrox Odyssey Xpro+ includes a configurable co-processor FPGA. This additional co-processor is based on the Altera® Stratix® II family of pin-compatible FPGA devices[4] and includes a bank of QDRII SRAM, which delivers an aggregate memory bandwidth of 4 GB/sec (i.e., 2 GB/sec input and 2 GB/sec output). Data to and from the co-processor FPGA travels through two ports with a combined capacity of 2 GB/sec. Histogram, LUT mapping and warping are just a sample of the operations accelerated by the co-processor FPGA.

freescale™ G4 PowerPC™ microprocessor

The CPU that controls activities on the Matrox Odyssey Xpro+ and performs operations not supported by the PA or co-processor FPGA is the freescale™ G4 PowerPC™ microprocessor. The G4 combines the best features of a general purpose CPU and a DSP, and provides top performance at a given clock rate. The G4 is also backed by freescale™'s solid migration path for increased performance, all the while maintaining code compatibility.

The G4 incorporates a powerful 32-bit superscalar RISC and AltiVec™ technology's 128-bit vector execution unit. 512 KB of internal L2 cache help sustain maximum processor performance. A 64-bit MPX bus offers efficient access to main memory and provides a sustained bandwidth close to its theoretical maximum of 1.3 GB per second.

AltiVec™ technology is specifically designed to meet the heavy computational requirements of applications such as video and image processing. This technology consists of a high-performance parallel processing engine for vector data. It uses the SIMD (single instruction, multiple data) model to process, in parallel, up to 16 pixels per cycle. It delivers a peak processing power of over 20 billion 8-bit MACs per second or over 10 billion 32-bit floating point operations per second when running at 1.4 GHz. Additionally, AltiVec™ technology operates concurrently with other execution units within the G4.

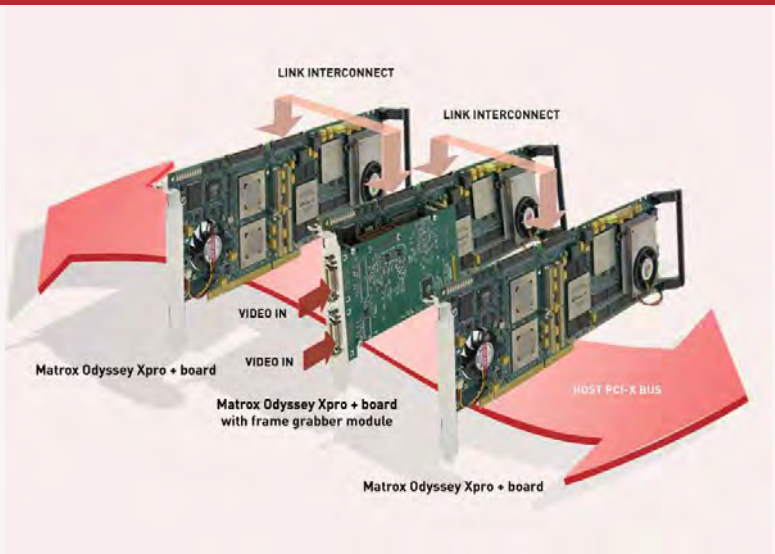
Lightning fast connectivity

PCI-X® is the fabric used on the Matrox Odyssey Xpro+ to connect a processing node to other processing nodes and PMC devices including an optional frame grabber module. It also connects the Matrox Odyssey Xpro+ to the host PC and display. PCI-X® is a high-performance backwards-compatible enhancement to the conventional PCI bus specification. Version 1.0 of PCI-X® specifies a 64-bit physical connection running at speeds of up to 133MHz resulting in a peak bandwidth of up to 1 GB per second. The Matrox System Interface Bridge (SIB), a four-port PCI-X® router custom designed by Matrox Imaging, handles the PCI-X® connections on the Matrox Odyssey Xpro+.

The Matrox Odyssey Xpro+ includes a pair of link ports dedicated to interconnecting multiple boards. The link ports provide point-to-point PCI-X® connections delivering up to 1 GB per second of bandwidth. They off-load the host PC bus by carrying video and message streams (see Matrox Oasis ASIC section) between boards. Video and message streams can be broadcasted or routed to specific processing nodes. A Matrox Odyssey Xpro+ configuration with multiple boards can be programmed to implement a variety of processing topologies, such as parallel, round robin and pipeline. Parallel topology consists of each processing node operating on a different part of a single image. Round robin topology consists of each processing node operating on a successive image. Pipeline topology consists of each processing node performing a distinct operation on a single image.

These topologies can be combined and apply to applications with a single or multiple video sources. In all cases, the processing capabilities of a multi-board system scale-up in a complete linear fashion as each additional node includes a dedicated bank of memory. This flexibility enables the Matrox Odyssey Xpro+ to handle any application requirements today and in the future.

Dedicated board-to-board interconnects



Flash EEPROM for full autonomy

Matrox Odyssey Xpro+ has a flash EEPROM that stores the G4 PowerPC™ boot sequence, system initialization parameters and a debugging utility. It can also be used to store the operating system and application program in order to implement a truly autonomous system from power-up.

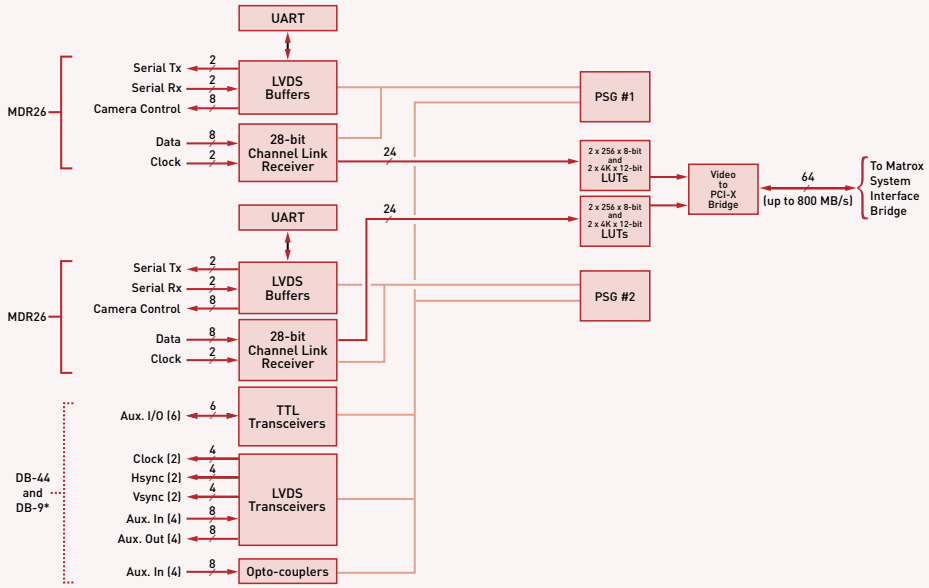
Frame grabbers to match

A standard PCI mezzanine card (PMC) site located on the Matrox Odyssey Xpro+ board allows the addition of a Camera Link® or analog frame grabber module[5]. These frame grabber modules enable the Matrox Odyssey Xpro+ to capture from the majority of area or line scan video sources.

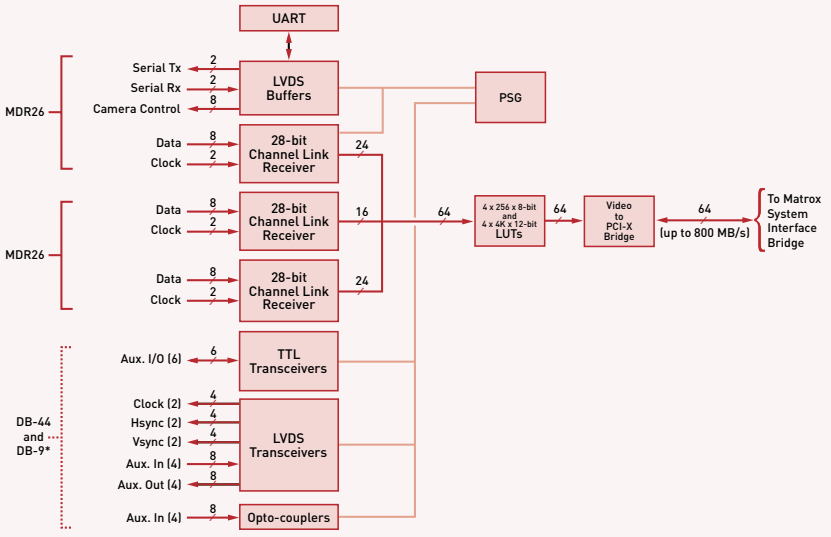
Camera Link® frame grabber module

The Camera Link® frame grabber module is available in one of two factory-configured versions. The dual-Base version enables simultaneous acquisition from two completely independent Camera Link® video sources utilizing the Base configuration[6]. The single-Full configuration acquires from a single Camera Link® video source utilizing the Base, Medium or Full configuration[6]. Both versions can operate at full Camera Link® speed and include an internal video generator for troubleshooting installation and operation.

Camera Link® module - dual Base version



Camera Link® module - single Full version



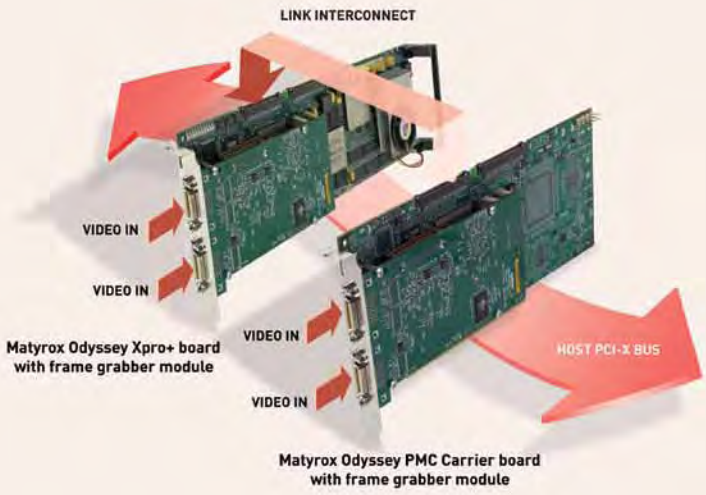
Analog frame grabber module

The analog frame grabber module has four completely independent inputs, each capable of high frequency and high fidelity video capture. In addition to being able to simultaneously acquire from four single-tap video sources, the inputs can be combined to simultaneously acquire from two dual-tap video sources or one RGB and one single-tap video source. The inputs can also be combined to simultaneously acquire from two video sources at double the nominal acquisition rate. The analog frame grabber module also includes an internal video generator for troubleshooting installation and operation.

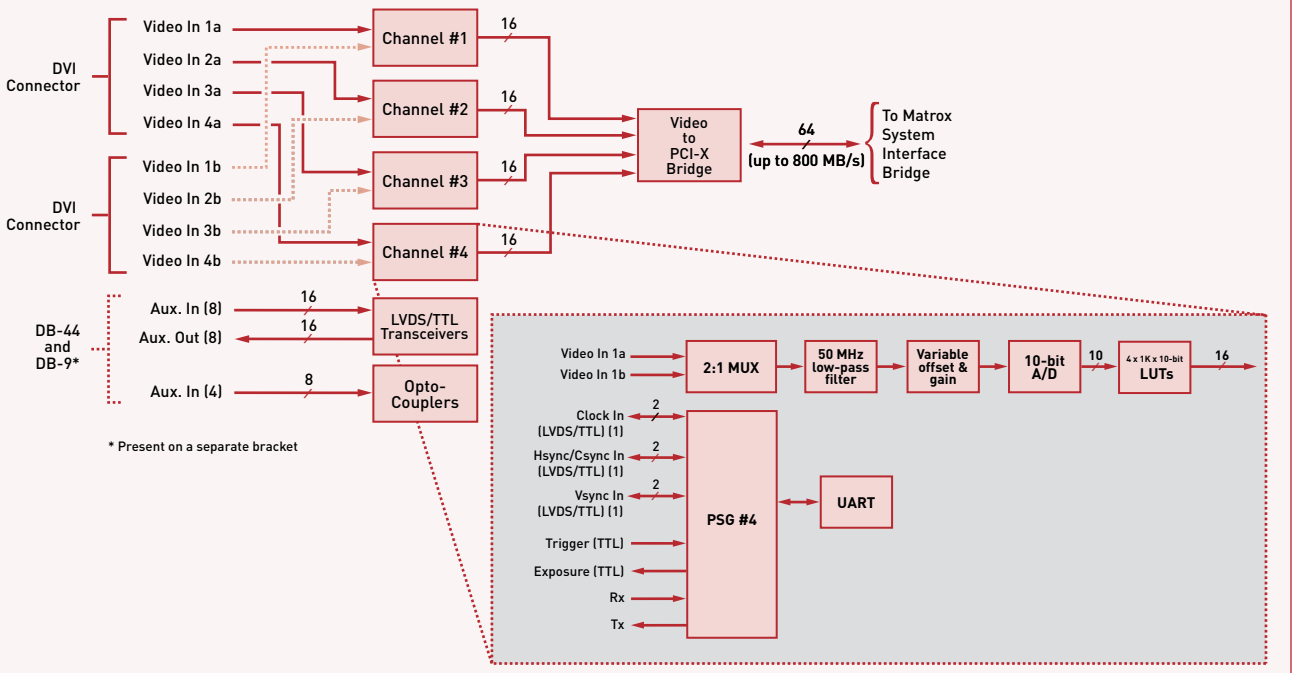
Adding frame grabber modules

An additional frame grabber module can be added to a Matrox Odyssey Xpro+ board by way of the Matrox Odyssey PMC carrier board. The Matrox Odyssey PMC carrier board occupies an additional PCI/PCI-X® slot and features a PMC site, which hosts a frame grabber module. The frame grabber module interacts with a Matrox Odyssey Xpro+ board over the link ports provided on the Matrox Odyssey PMC carrier board (see Lightning fast connectivity section).

Matrox Odyssey PMC carrier board



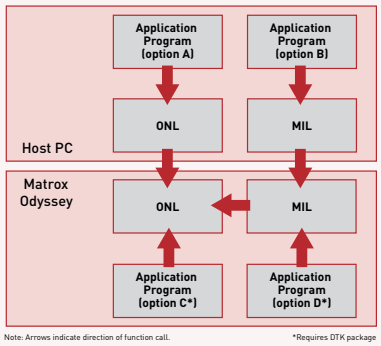
Analog module



All-encompassing programming environment

The Matrox Odyssey Xpro+ offers the developer a choice of application programming interfaces (APIs) and programming models. Application developers can program the board using the Matrox Imaging Library or Matrox Odyssey Native Library, each with royalty-free run-time environments[1]. The application program can run on the host PC to remotely control the Matrox Odyssey Xpro+ (i.e., options A and B) or it can be made to run entirely on the Matrox Odyssey Xpro+ (i.e., options C and D).

Software environment



Matrox Imaging Library (MIL)

MIL is a complete and easy-to-use programming library for image capture, processing, analysis, display and archiving that supports the complete line of existing and future Matrox Imaging hardware. MIL's field-proven processing and analysis functions include point-to-point, statistics, filtering, morphology, geometric transformations, FFT, segmentation, pattern recognition, blob analysis, edge extraction and analysis, measurement, character recognition, 1D and 2D code reading, calibration, and JPEG/JPEG2000 image compression. These functions run on the Matrox Odyssey Xpro+ and are fully optimized for the G4 PowerPC™ and PA.

MIL for the Matrox Odyssey Xpro+ is carefully tuned to exhibit low function call overheads, maximizing application efficiency and performance. A MIL-based application program can run efficiently on a single processing node or across multiple processing nodes. MIL provides transparent image display management with automatic tracking and updating of image display windows at live video rates. MIL also allows for image display in a user-specified window. In addition, MIL supports live display of multiple video streams using multiple independent windows or a single mosaic window. Moreover, MIL provides non-destructive graphics overlay, suppression of tearing artifacts and filling the display area at live video rates. All of these features are performed with little or no host CPU intervention when using the appropriate graphics hardware. Refer to the MIL datasheet for more information.

Odyssey Native Library (ONL)

ONL is an easy-to-use programming library specific to the Matrox Odyssey family of vision processor boards. The programming interface is compatible with the Matrox Genesis family of vision processor boards. Aside from video capture and system control including multiple processing nodes, ONL includes functions for image processing, normalized grayscale correlation-based pattern recognition, blob analysis and JPEG compression. These functions are fully optimized to exploit the power of the G4 PowerPC™ and PA. ONL functions exhibit the lowest call overheads.

Programming models

Application programs for the Matrox Odyssey Xpro+ can run in a host-driven or fully embedded mode. In the host-driven mode, the application program runs on the CPU of the host PC and remotely sends commands to the Matrox Odyssey Xpro+ for execution. The host-driven mode is the easiest to implement but it may be subject to the lack of determinism of the host PC platform. In the fully embedded mode, the application program runs directly on the G4 PowerPC™. The application program has little or no interaction with the host PC platform, ensuring deterministic behavior. Using the fully embedded mode requires the Matrox Odyssey Developer's Toolkit.

Matrox Odyssey Developer's Toolkit

The Matrox Odyssey Developer's Toolkit (DTK) allows a developer to extract the full power of the Matrox Odyssey Xpro+. In addition to giving the means to run a MIL and/or ONL-based application program directly on the G4 PowerPC™, the Matrox Odyssey DTK lets a developer further optimize an algorithm by merging ONL functions to reduce main memory I/O bottlenecks.

The Matrox Odyssey DTK also allows developers to write custom G4 PowerPC™ and PA functions. Custom G4 PowerPC™ code is written entirely in C/C++ including optimizations for AltiVec™ technology. AltiVec™ technology is programmed through C language extensions and intrinsic functions. No exotic assembly code is required. Custom PA code is done through a low-level API and pseudo-assembly language. Refer to the Matrox Odyssey Developer's Toolkit datasheet for more information.

Utilities

Bundled with the MIL and ONL software development kit is the Matrox Intellicam camera configuration utility. Matrox Intellicam is a Windows®-based program that lets users interactively configure the frame grabber modules to capture from a variety of video sources. Also included is an interactive system configuration and debugging utility that incorporates a multi-board configuration tool, memory and command viewer, performance monitor and system diagnostic tool.

Operating system support

Supported host environments for the Matrox Odyssey Xpro+ are 32/64-bit Microsoft® Windows® XP/Vista®/7 and 32-bit Linux®. The G4 PowerPC runs an off-the-shelf RTOS with a very small footprint and fast response to task switches and interrupts.

Co-processor FPGA configurations

Included with the MIL/ONL software development kits are ready-made configurations for the co-processor FPGA that implement a variety of image processing functions. Custom configurations can also be created on demand and upon evaluation.

Specifications

Processor board

- PCI/PCI-X® long card with 3.3V 64-bit card edge connector
- 1.4 GHz MPC7448 (167 MHz MPX bus)
- 1 GB of 167 MHz DDR SDRAM main memory
- customizable co-processor FPGA
  - Altera® Stratix® II family[4]
  - 16 or 32 MB QDRII SRAM
- 16 MB flash EEPROM
- 64-bit 33/66/100/133 MHz 3.3V PMC site
- two 64-bit 33/66 MHz 3.3V PCI and 64-bit 66/100/133 MHz PCI-X® dedicated links
- 64-bit 33/66 MHz 3.3V PCI and 64-bit 66/100/133 MHz PCI-X® host interface

Camera Link® frame grabber module[5]

- two factory configured versions
  - two independent Camera Link® Base ports[6] (dual-Base)
  - single Camera Link® Base/Medium/Full port[6] (single-Full)
- Channel Link™ speed of up to 85 MHz
- supports frame and line-scan video sources
- four 256 x 8-bit and four 4K x 12-bit LUTs
- six TTL configurable auxiliary I/Os
- four LVDS configurable auxiliary inputs
- four LVDS configurable auxiliary outputs
- two separate LVDS pixel clock, hsync and vsync outputs
- four opto-isolated configurable auxiliary inputs
- internal video generator for diagnostics

Analog frame grabber module[5]

- four independent video inputs with
  - 2:1 mux
  - AC or DC coupling
  - 50 MHz low pass filter with bypass
  - variable gain amplifier and adjustable references
  - 10-bit A/D with sampling rate up to 100 MHz
  - SNR of 50.4 dB[7]
  - pixel jitter of ± 4.3 ns[8]
  - adjustable clock phase (256 steps with 0.5 ns resolution)
  - four 1K x 10-bit LUTs
  - LVDS/TTL pixel clock, hsync/csync, and vsync inputs or outputs
  - TTL trigger input and exposure output
  - serial communication port
- inputs can be combined to acquire from
  - component RGB video source
  - two dual-tap monochrome video sources
  - two monochrome video sources at up to 200 MHz
- supports frame and line-scan video sources
- eight TTL/LVDS configurable auxiliary inputs
- eight TTL/LVDS configurable auxiliary outputs
- four opto-isolated auxiliary inputs
- PROM for storing calibration parameters
- internal video generator for diagnostics

PMC carrier board

- PCI/PCI-X® card with universal 64-bit card edge connector (only draws power)
- 64-bit 33/66/100/133 MHz 3.3V PMC site
- two 64-bit 33/66/ MHz 3.3V PCI and 64-bit 66/100/133 MHz PCI-X dedicated links

Dimensions and environmental information

- 31.2 L x 10.7 H x 1.73 W cm (12.3" x 4.2" x 0.68") from bottom edge of goldfinger to top edge of board, and without bracket and retainer[9]
- power consumption (typical)
  - 11.2A @ 3.3V or 36.96W, 5.6A @ 5V or 28.0W, or 64.96W total for processor board
  - 1.04A @ 3.3V or 3.4W, 0.15A @ 5V or 0.8W, or 4.2W total for PMC carrier board
  - 1.21A @ 3.3V or 4W, 0.92A @ 5V or 4.6W, 0.33A @ 12V or 4W, or 12.6W total for analog frame grabber module
  - 0.75A @ 3.3V or 2.5W, 0.3A @ 5V or 1.5W, or 4W total for Camera Link® frame grabber module
  - 0.97A @ 3.3V or 3.2W, 0.24A @ 5V or 1.2W, or 4.4W total for LVDS/RS-422 frame grabber module
- operating temperature: 0° C to 55° C (32° F to 131° F)
- ventilation requirements: 150 LFM (linear feet per minute) over board(s)
- relative humidity: up to 95% (non-condensing)
- FCC class A pending
- CE class A pending
- RoHS-compliant

Software drivers

- host drivers for 32/64-bit Microsoft® Windows® XP/Vista®/7 and 32-bit Linux®

Ordering Information

Boards

Part number	Description
O+ 141G 06316 xxxx*	Scalable PCI-X® vision processor board with 1.4 GHz MPC7448, 1 GB DDR SDRAM, EP2S60...C3 FPGA with 16 MB QDRII SRAM and optional frame grabber module.
OCB xxxx*	PMC carrier board with optional frame grabber module.
OLPIC*	Link port interconnect board.

NOTE: Remove xxxx for no frame grabber module or replace with suffix below for appropriate frame grabber module. Frame grabber modules are not available separately.

...SFCL...	Single-FULL Camera Link® frame grabber module and cable adapter board.
...DBCL...	Dual BASE Camera Link® frame grabber module and cable adapter board.
...QHAL...	Quad-input high-frequency analog frame grabber module and cable adapter board (LVDS aux I/O).

Software

Part number	Description
MIL 9 WIN ODY	MIL 9 development toolkit for Matrox Odyssey running under 32/64-bit Windows® XP/Vista/7. Includes DVDs with MIL, ONL, Intellicam, Inspector (32-bit), Matrox display drivers and online documentation.
MIL 9 LNX	MIL 9 development toolkit for 32-bit Linux®. Includes DVD with MIL, ONL and online documentation. Also requires MIL9WINODY.
MIL 9 DTK WIN	Add-on to MIL 9 development toolkit for 32/64-bit Windows® XP / Vista®/7. Required for writing code for Matrox Odyssey's Pixel Accelerator (PA) and PowerPC™. Also requires Code Warrior™ for Power PC™ Embedded Systems.

Software Maintenance Program

Included in the original purchase price of the Matrox Odyssey SDK and DTK, it entitles registered users to one year of technical support and free updates.

Part number	Description
MIL MAINTENANCE	One year program extension per developer.

Cables

Part number	Description
DVI-TO-8BNC/O	8' or 2.4 m, DVI to 8 BNCs and open end cable for analog frame grabber module (requires customization).
DBHD100-TO-OPEN	3 m (10') high density DB-100 to open end cable for LVDS/RS-422 frame grabber module (requires customization).

Cables

Camera Link® cables available from camera manufacturer, 3M Interconnect Solutions (www.3m.com), Intercon1 (www.nortechsys.com/intercon) or other third parties.
Cables for cable adapter boards available from third parties.

Notes:

1. MIL for Matrox Odyssey includes MIL for IA32 (host PC), which requires an additional development or run-time license.
2. Only one source buffer for MAC unit.
3. Billion operations per second.
4. EP2S60 and EP2S130 devices.
5. Frame grabber modules only work with Matrox Odyssey Xpro+.
6. Refer to Camera Link® specification for more information.
7. Measured with 50MHz low pass filter.
8. Measured with a horizontal reference signal at 15.7 kHz (RS-170).
9. 24.8L x 10.7H x 1.9W cm (4.8" x 4.2" x 0.75") for PMC carrier board.