Frame grabbers

Matrox **Helios eA/XA**

High performance analog frame grabber with powerful pre-processing capabilities.

Key features

- x4 PCIe™ (eA) or PCI-X® (XA) long card
- four fully independent inputs
- 10-bit A/D converters
- sampling rate up to 160 MHz
- video synchronization and PLL lock detection
- 256 MB of DDR SDRAM memory
- over 5 GB per second of memory bandwidth
- powerful pre-processing core capable of up to 100 BOPS[1]
- up to 1 GB per second of I/O bandwidth to host PC
- serial communication ports can be mapped as PC COM ports
- support for rotary encoders with quadrature output
- programmed using Matrox Imaging Library (MIL) sold separately
- supports 32/64-bit Microsoft® Windows® XP/Vista®/7 and 32/64-bit Linux®
- royalty-free redistribution of MIL's image processing module

Exceptional video capture rates and more

Matrox Helios eA/XA is the new standard in high-performance analog frame grabbers. It fully exploits PCIe™/PCI-X® technology to deliver unprecedented video capture rates for a single-board solution and can easily accommodate the most demanding analog video sources. A custom ASIC, designed by Matrox, combines a PCI-X controller with a powerful processor core to alleviate the host CPU from image formatting and pre-processing tasks. These features provide the Matrox Helios eA/XA with the power and flexibility needed for vision applications of today and tomorrow.

High frequency and high fidelity analog frame grabber

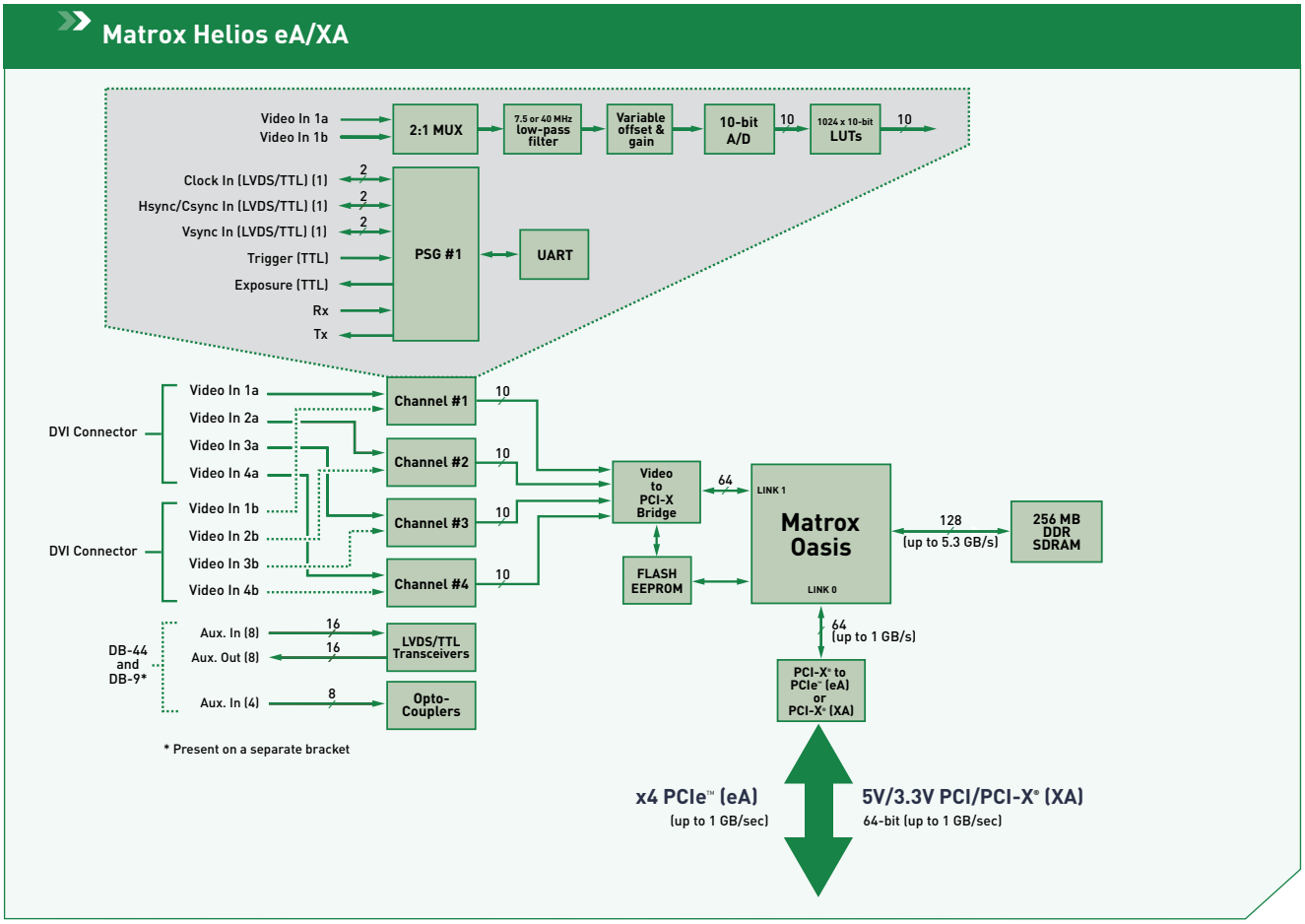
The Matrox Helios eA/XA has four completely independent inputs, each capable of high frequency and high fidelity video capture. In addition to being able to simultaneously acquire from up to four single-tap video sources, the inputs can be combined to simultaneously acquire from two dual-tap video sources or one RGB video source. The inputs can also be combined to simultaneously acquire from two video sources at twice the nominal acquisition rate. Each input of the Matrox Helios eA/XA features circuitry to monitor the presence of a video (synchronization) signal and status of the phase-locked loop. The Matrox Helios eA/XA also includes an internal video generator for troubleshooting installation and operation.

Choice of high-performance host bus interfaces

Four lane (x4) PCIe™ and PCI-X® are the interfaces used to connect to the host PC on the Matrox Helios eA and Matrox Helios XA boards respectively. PCIe™ is the follow-on to conventional PCI and PCI-X®. Version 1.x of PCIe™ operates at 2.5 GHz to deliver a peak bandwidth of 1GB/sec over a x4 implementation. PCI-X® is a high-performance backwards-compatible enhancement to conventional PCI. Version 1.0a of PCI-X® specifies a 64-bit physical connection running at speeds of up to 133 MHz resulting in a peak bandwidth of up to 1 GB per second.

MATROX IMAGING

Matrox Helios eA/XA



State-of-the-art Matrox Oasis ASIC

The Matrox Imaging designed Oasis ASIC is the pivotal component of the Matrox Helios eA/XA. A high-density chip, the Matrox Oasis integrates a Links Controller, main memory controller and Pixel Accelerator.

Pixel Accelerator

The Pixel Accelerator (PA) is a parallel processor core, which considerably accelerates neighborhood, point-to-point and LUT mapping operations. It consists of an array of 64 processing elements all working in parallel. Each processing element has a multiply-accumulate (MAC) unit and an arithmetic-logic unit (ALU).

The MAC unit is capable of performing a single 16-bit by 16-bit, two 8-bit by 16-bit or four 8-bit by 8-bit multiplies with 40-bit accumulation per cycle for convolution operations.The 40-bit accumulator guarantees no overflow situation for a 16 by 16 kernel with 16-bit coefficients and data. In addition, the PA architecture allows symmetrical kernels to be processed four times faster. The MAC unit is also able to perform up to four minimum or maximum operations per cycle for grayscale morphology operations.

The ALU can execute a wide variety of arithmetic and logical operations. It can be programmed to execute a sequence of 256 instructions per pixel at one instruction per cycle reducing the amount of memory accesses and further accelerating memory I/O-bound sequences. The PA can accept up to four source buffers[2] and output to four destination buffers allowing several operations to be performed at once or in a single pass (i.e., four images can be averaged in one pass). Operating at a core frequency of 167 MHz enables the PA to carry out up to 100 BOPS[1] (i.e., process over two billion pixels per second).

Memory controller

The Matrox Oasis includes a very efficient main memory controller for managing the 128-bit wide interface to DDR SDRAM memory. Operating at 167 MHz, the DDR SDRAM memory and controller combine to deliver a memory bandwidth in excess of 5 GB
per second. Such ample memory bandwidth allows the Matrox Helios eA/XA to comfortably handle demanding video I/O while maintaining PA performance even for memory I/O-bound operations.

Links Controller

The Links Controller (LINX) is the router that manages all data movement within the Matrox Helios eA/XA. It oversees the transfer of image data from the frame grabber section to onboard memory for pre-processing and from onboard memory to the host PC including display. Image data can be subject to various formatting operations including plane separation on input and merging on output, input cropping, input and output sub-sampling (1 to 16), and independent control of horizontal and vertical scanning direction. The latter is particularly useful for reconstructing a proper image from a camera whose readout requires multiple taps, each with different scanning directions.

Field-proven application development software

Matrox Helios eA/XA is supported by the Matrox Imaging Library (MIL), a comprehensive collection of software tools for developing industrial imaging applications. MIL features interactive software and programming functions for image capture, processing, analysis, annotation, display and archiving. These tools are designed to enhance productivity, thereby reducing the time and effort required to bring your solution to market. Refer to the MIL datasheet for more information.

MIL's image processing module, when used with the Matrox Helios eA/XA, comes with royalty-free redistribution rights. The image processing module, which includes functions for basic arithmetic, logic, LUT mapping, per pixel gain and offset, morphology, spatial filtering, statistics, temporal filtering and threshold, is fully optimized for the PA[3]. Support for custom PA functions is also available on demand and upon evaluation.

Specifications

Hardware

- x4 PCIe™ long card or PCI/PCI-X® long card with universal 64-bit card edge connector (64-bit 33/66 MHz 5/3.3V PCI and 64-bit 66/100/133 MHz PCI-X)
- 256 MB of 167 MHz DDR SDRAM main memory
- four independent analog video inputs with
  - 2:1 mux
  - AC or DC coupling
  - selectable low pass filter: 7.5 MHz or 40 MHz
  - variable gain amplifier and adjustable references
  - 10-bit A/D with sampling rate up to 80 MHz
  - SNR of 51.7 dB[4]
  - pixel jitter of ±2.3ns[5]
  - adjustable clock phase (256 steps with 0.5 ns resolution)
  - four 1K x 10-bit LUTs
  - LVDS/TTL pixel clock, hsync/csync and vsync inputs or outputs
  - TTL trigger input and exposure output
  - RS-232 serial port that can be mapped as a PC COM port
- inputs can be combined to acquire from
  - component RGB video source
  - two dual-tap monochrome video sources
  - two monochrome video sources at up to 160 MHz
- supports frame and line-scan video sources
- eight TTL/LVDS configurable auxiliary inputs
- eight TTL/LVDS configurable auxiliary outputs
- four opto-isolated auxiliary inputs
- PROM for storing calibration parameters
- internal video generator for diagnostics

Environmental information

- 31.2 L x 10.7 H x 1.73 W cm (12.3" x 4.2" x 0.68") from bottom edge of the board, and without bracket and retainer
- power consumption (typical): 2A @ 3.3V or 6.6W, 1.1A @ 5.0V or 5.5W, 0.42A @ 12V or 5.04W, or 17.14W total
- operating temperature: 0°C to 55° C (32° F to 131° F)
- ventilation requirements: 50 LFM (linear feet per minute) over board(s)
- relative humidity: up to 95% (non-condensing)
- FCC class A
- CE class A
- RoHS-compliant

Software drivers

- Matrox Imaging Library (MIL) drivers for 32/64-bit Microsoft® Windows® XP/Vista®/7
- MIL drivers for 32/64-bit Linux®

Ordering Information

Hardware

Part number	Description
HEL 2M QHAL*	PCI-X® analog frame grabber with four independent inputs, 256 MB DDR SDRAM and cable adapter board (LVDS aux.I/O).
HEL 2M QHAL E*	x4 PCIe™ analog frame grabber with four independent inputs, 256 MB DDR SDRAM and cable adapter board (LVDS aux.I/O).

Software

Refer to MIL datasheet.

Cables

Part number	Description
DVI-TO-8BNC/0	8' or 2.4 m cable, DVI to 8 BNCs and open end (requires customization).

Notes:

1. Billion operations per second.
2. Only one source buffer for MAC unit.
3. MbufBayer (bilinear interpolation), MimArithMultiple (M_OFFSET_GAIN, M_WEIGHTED_AVERAGE, M_MULTIPLY_ACCUMULATE), MimArith (M_ADD, M_ADD_CONST, M_SUB, M_SUB_CONST, M_SUB_ABS, M_MULT, M_MULT_CONST, M_CONST_SUB, M_AND, M_NAND, M_OR,M_XOR, M_NOR, M_XNOR, M_NOT, M_AND_CONST, M_NAND_CONST, M_OR_CONST, M_XOR_CONST, M_NOR_CONST, M_XNOR_CONST, M_NEG,M_ABS, M_MIN, M_MIN_CONST, M_MAX, M_MAX_CONST), MimResize (with specific factors), MimDilate(), MimErode(), MimThin(), MimThick(), MimDistance(), MimConnectMap(), MimMorphic (M_DILATE, M_ERODE, M_THICK, M_THIN, M_MATCH), MimConvolve (M_SMOOTH, M_SHARPEN, M_VERT_EDGE, M_HORIZ_EDGE, M_LAPLACIAN_EDGE, M_EDGE_DETECT), MimLutMap(8-bit), MimShift(), MimBinarize(), MimClip(), MimConvert (M_YUV16_TO_RGB, M_RGB_TO_YUV16, M_RGB_TO_L, M_L_TO_RGB,M_RGB_TO_Y), MimFlip(), MimFindExtreme(), MimCountDifference()and ActiveMIL equivalents.
4. Measured with 40MHz low pass filter.
5. Measured with a horizontal reference signal at 15.7KHz (RS-170).

matrox®